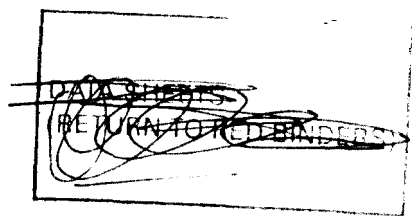
A100x

VXI bus

HP *75000* SERIES *C*

Model D20
Digital Functional Test System

Using Multiple Mainframes
Installation and Programming Guide



HEWLETT PACKARD

E I493-90024
E0692

Manual Part Number: E1493-90024
Microfiche Part Number: E1493-99024

Printed: June 1992 Edition 1
Printed in U.S.A.

Contents

Using Multiple Mainframes

Introduction

This installation and programming guide gives you information for configuring multiple mainframe systems. You can configure multiple mainframe systems using an expanded **HP-IB** configuration or using VXI-MXI **Bus** Extender Modules. If your multiple mainframe system uses the VXI-MXI Bus, refer to your HP E1482 User's Manual for hardware configuration and addressing information. Chapter 2 of this manual provides programming information for **a** VXI-MXIbus configured system.

NOTE

Refer to the HP E1482 User's Manual for hardware configuration and addressing information if your multiple mainframe system uses VXI-MXI Bus Extender Modules instead of the expanded HP-IB mainframe configuration described in this document. Chapter **2** *of this guide provides VXI-MXIbus programming information for a multiple mainframe system.*

Other Installation References

- Refer to the HP 75000 Model D20 "Hardware Installation Guide" for more information on logical addresses, card installation, pod installation, and external wiring to the device under test.
- Refer to the "C-Size VXIbus Systems Installation and Getting Started Guide" for mainframe powering-up and getting started information.
- **If you have the HP E1496 Test Development Software,** refer to **its** Software Installation Guide.
- **If you DO NOT have the HP E1496 Test Development Software,** refer to the "Downloading Device Drivers Installation Note" for information on how to load the Model D20 firmware from the file named "DIGITAL" on the firmware disk.

Do Not Discard This Document

You may need this document when making future changes to the existing hardware configuration. Store this guide in your system documentation binder.

Chapter 1
Expanded HP-IB Configuration

Installation: Expanded HP-IB Configuration

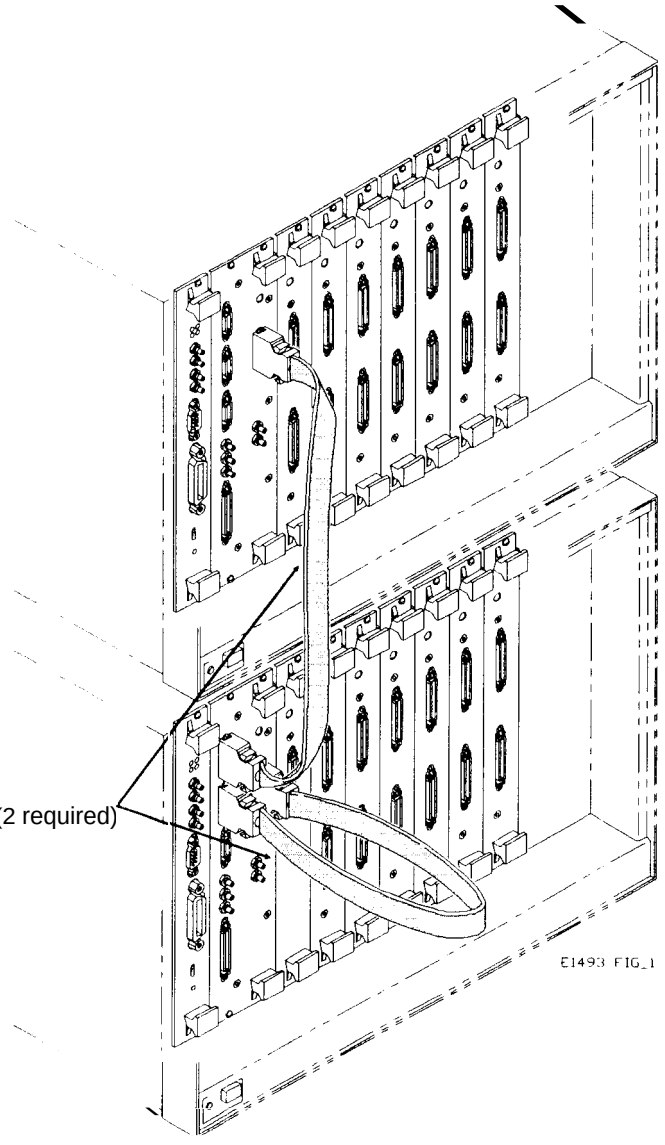
You can synchronize multiple instruments operating in multiple mainframes using the "Expanded **HP-IB** Configuration". In this configuration, one frame is the master and the other frames are slaves. Figure 1 shows the connections for **2** mainframes and Figure 2 shows connections for **3** mainframes.

Installation requirements **for** this configuration are:

- Each mainframe must have a **VXI** resource manager and slot **0** device (e.g. HP E1405/1406 Command Module).
- Each mainframe must have a different HP-IB primary address (instrument secondary addresses can be the same). For example, when using **3** frames, the HP-IB addresses might be: 70717,70817, and 70917.
- You must use the longer master/slave cable (HP E1450-61603) on every frame including the master.

CAUTION

DO NOT use any short master/slave cables in a multiple frame installation; the instruments will no longer be within specifications. Use only the long master/slave cables (HP E1450-61603). Having all master/slave cables the same length results in equal propagation delays through each cable.



HP E1450-61603 (2 required)

Slave Frame Logical Addresses:

- HP E1450 = 136 (Secondary Address = 17)
- HP E1451 #1 = 137
- HP E1451 #2 = 138

- HP E1451 #6 = 142
- HP E1452 = 143

HP-IB Address = 70817

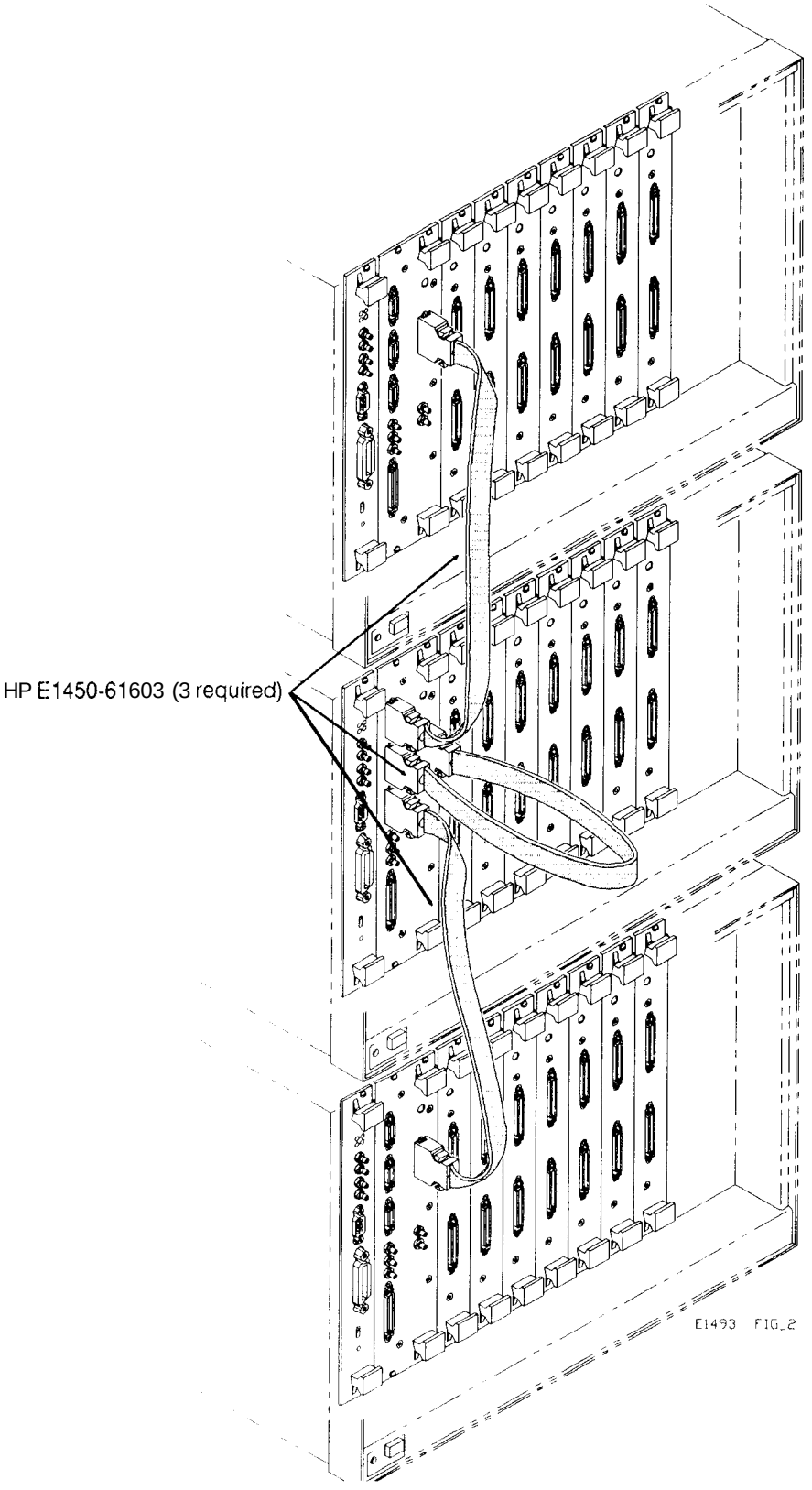
Master Frame Logical Addresses:

- HP E1450 = 136 (Secondary Address = 17)
- HP E1451 #1 = 137
- HP E1451 #2 = 138

- HP E1451 #6 = 142
- HP E1452 = 143

HP-IB Address = 70917

Figure 1. Expanded HP-IB Configuration (2 Frames)



Slave #1 Frame Logical Addresses:

- HP E1450 = 136 (Secondary Address = 17)
- HP E1451 #1 = 137
- HP E1451 #2 = 138

- HP E1451 #6 = 142
- HP E1452 = 143

HP-IB Address = 70717

Master Frame Logical Addresses:

- HP E1450 = 136 (Secondary Address = 17)
- HP E1451 #1 = 137
- HP E1451 #2 = 138

- HP E1451 #6 = 142
- HP E1452 = 143

HP-IB Address = 70917

Slave #2 Frame Logical Addresses:

- HP E1450 = 136 (Secondary Address = 17)
- HP E1451 #1 = 137
- HP E1451 #2 = 138

- HP E1451 #6 = 142
- HP E1452 = 143

HP-IB Address = 70817

Figure 2. Expanded HP-IB Configuration (3 Frames)

Programming: Expanded HP-IB Configuration

When using the expanded HP-IB configuration, all instruments must have identical programs. This means that the number of vectors in the sequences, the number of subcycles in the timing cycles, and the timing resolution must be identical for all instruments. The stimulus/response patterns and control output waveforms, however, can be different for each instrument (as long as the same number of vectors is used for each instrument).

Synchronization between the frames is ensured by controlling the reference oscillator for all frames. That is, you must disable the reference oscillators for all frames, run the programs for all frames, and then enable the oscillators. When all of the oscillators have been enabled, sequence execution begins for all frames simultaneously.

When in this configuration, the master instrument is the source for all triggering, conditions ("Q" inputs), and the End-If-Ready signal. That is, when a trigger, condition, or End-If-Ready is used in the sequences, when the event occurs at the master instrument, it satisfies the event requirement for all instruments. The trigger, "Q", and End-If-Ready input connectors for the slaves are disabled.

Example, Synchronizing Multiple Instruments

The example on the following pages uses three instruments in three mainframes as shown in Figure **2.** The instrument at HP-IB address 70917 is the master; addresses 70717 and 70817 are the slaves. The identical sequences, timing cycles, and resolutions are used for each instrument. Different stimulus sequence patterns are used for each instrument. When initially set up, the reference oscillators for all instruments are disabled (DIAGnostic:OSCillator OFF command). After running all three programs, the DIAGnostic:OSCillator ON command is sent to each instrument and enables the reference oscillator. When all three oscillators are enabled, all three sequences begin execution simultaneously.

```
10   !RE-SAVE "MULTINST"                                  !Delete "!" to save file
20   Dft = 70717                                          !Slave 1 address
21   ! - - - - - - - - - - Set Up Each Instrument- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
30   LOOP
40   EXIT IF Dft = 71017
50     OUTPUT Dft;"*RST"                                  !Sets instrument to a known condition
60     OUTPUT Dft;"SEQ:DEL:ALL"                           !Delete all previous sequences
70     OUTPUT Dft;"SEQ:DEF TEST_4,17"                     !Define sequence "TEST-4" containing 17 vectors
80     OUTPUT Dft;"SEQ TEST-4"                            !Select "TEST-4" sequerice
90     OUTPUT Dft;"GRO:DEL:ALL"                           !Delete all previous pin groups
100    OUTPUT Dft;"GRO:DEF ADDR_BUS,(@1(1,0))"            !"ADDR_BUS" group = ports 0/1 on left Pattern I/O
110    OUTPUT Dft;"GRO:DEF DATA-OUT,(@ (2,3))"            !"DATA_OUT" group = ports 213 on left Pattern I/O
120    OUTPUT Dft;"GRO ADDR_BUS"                          !Select pin group "ADDR_BUS"
130    OUTPUT Dft;"GRO:MODE STIM"                         !Set group to stimulus mode
140    OUTPUT Dft;"STIM:CLOC:SOUR INTO"                   !Use internal stimulus clock 0
150    OUTPUT Dft;"GRO DATA-0UT"                          !Select pin group "DATA-OUT'
160    OUTPUT Dft;"GRO:MODE STIM"                         !Set group to stimulus mode
170    OUTPUT Dft;"STIM:CLOC:SOUR INTO"                   !Use internal stimulus clock 0
180    OUTPUT Dft;"TIM:CYCL:DEL:ALL"                      !Delete all previous timing cycles
190    OUTPUT Dft;"TIM:CYCL:DEF TC_1,750"                 !Define timing cycle "TC_1" having 750 subcycles
200    OUTPUT Dft;"TIM:CYCL:SEQ:REP 0,17,TC_1"            !Assigns timing cycle "TC_1" to each vector
210    OUTPUT Dft;"TIM:RES 400e-6"                        !Each subcycle = 400us
220    OUTPUT Dft;"DIAG:OSC OFF"                          !Turn off reference oscillator
230    Dft = Dft + 100
240  END LOOP
241  ! - - - - - - - - - - Load Sequence Patterns & RUN Slave #1- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
250  OUTPUT 70717;"GRO ADDR_BUS"                          !Select pin group "ADDR_BUS"
260  OUTPUT 70717;"STIM:PATT:SEQ:PART 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,0" !Address pattern
270  OUTPUT 70717;"GRO DATA-OUT'                          !Select pin group "DATA-OUT'
280  OUTPUT 70717;"STIM:PATT:SEQ:PART 0,1,2,4,8,16,32,64,128,256,512,1024,2048,4096,8192,16384,
32768,0"                                                  !Load data pattern
290  OUTPUT 70717;"RUN"                                   !RUN command to slave #1 Frame
291  ! - - - - - - - - - - Load Sequence Patterns & RUN Slave #2 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
300  OUTPUT 70817;"GRO ADDR-BUS"                          !Select pin group "ADDR_BUS"
310  OUTPUT 70817;"STIM:PATT:SEQ:PART 0,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,0"
320  OUTPUT 70817;"GRO DATA-OUT"                          !Select pin group "DATA_OUT"
330  OUTPUT 70817;"STIM:PATT:SEQ:PART 0,1024,2048,4096,8192, 16384,32768,1,2,4,8,16,32,64,128,
256,512,0"                                                !Load data pattern
340  OUTPUT 70817;"RUN"                                   !RUN command to slave #2 Frame
341  ! - - - - - - - - - - Load Sequence Patterns & RUN Master - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
350  OUTPUT 70917;"GRO ADDR-BUS"                          !Select pin group "ADDR_BUS"
360  OUTPUT 70917;"STIM:PATT:SEQ:PART 0,16,15,14,13,12,11,10,9,8,7,6,5,4,3,2,1,0" !Address pattern
370  OUTPUT 70917;"GRO DATA-OUT'                          !Select pin group "DATA_OUT"
380  OUTPUT 70917;"STIM:PATT:SEQ:PART 0,32768,16384,8192,4096,2048,1024,512,256,128,64, 32,16,
8,4,2,1,0"                                                !Load data pattern
390  OUTPUT 70917;"RUN"                                   !RUN command to Master Frame
391  ! - - - - - - - - - - Enable Muster Timing Module Oscillator to begin Sequences - - - - - - - - - - - - - - - - - - - - -
400  OUTPUT 70917;"DIAG:OSC ON"                           !Enable master oscillator, begin sequences
410  END                                                  ! simultaneously in all three frames
```

Chapter 2
VXI-MXIbus Configuration

Installation: VXI-MXIbus Configuration

For very large test systems that require multiple mainframes, all modules in the mainframes can be treated as one instrument using the VXI-MXI Bus. Figure 3 shows an example of a three mainframe system configured with the VXI-MXI Bus. One frame is the master and the other frames are slaves. You can synchronize all three Timing Modules by connecting the master/slave cables as shown which makes the middle frame the master frame.

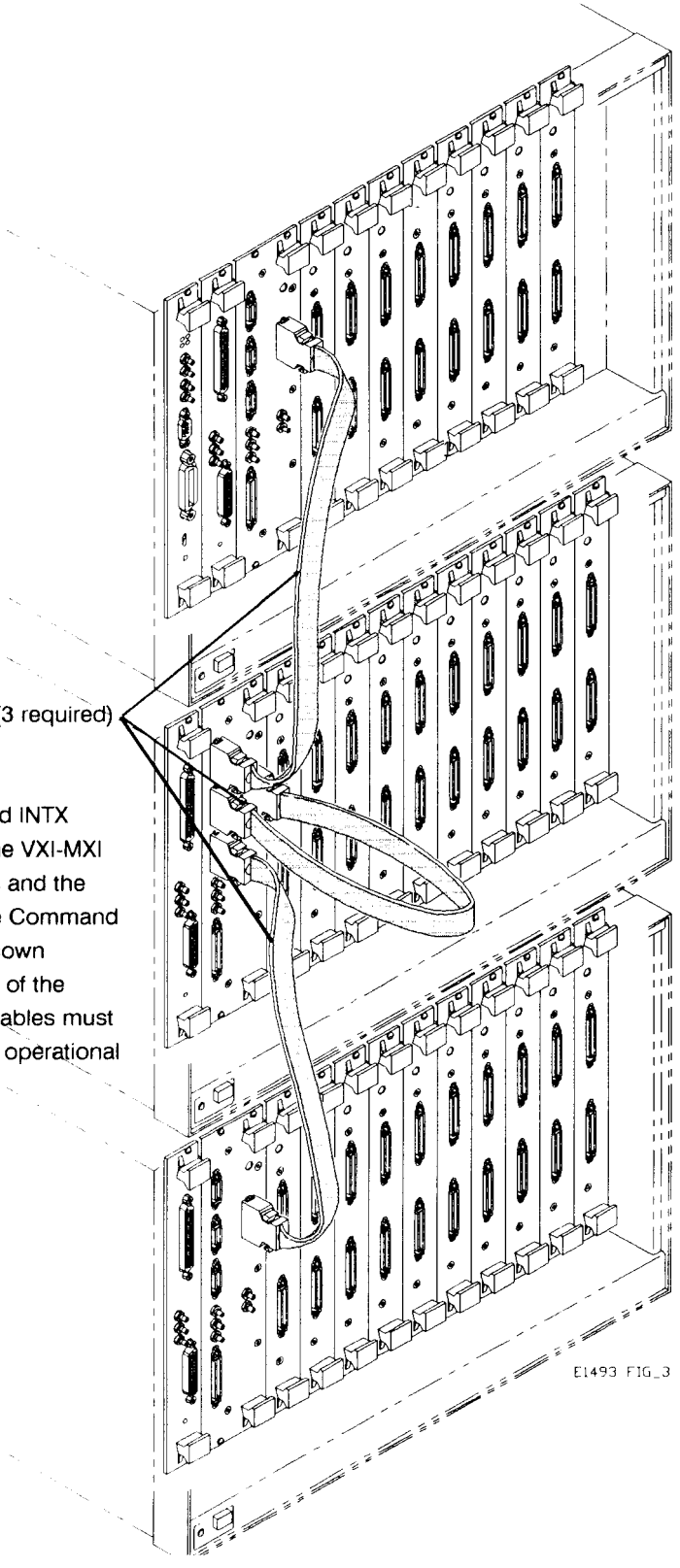
Installation requirements for this configuration are:

- The master frame is the middle mainframe to allow a master/slave cable connection to both slave mainframes. **CAUTION** The master/slave cable (HP E1450-61603) must be used on every frame including the master to maintain the same propagation delay from the master oscillator to all slave sections (including the master's own slave section). Timing specifications are invalid otherwise.
- The master timing module is the only timing module with valid trigger and Q lines.
- The master timing module is the timing module with the lowest logical address; slave timing modules must have a logical address greater than the master timing module.
- The VXI-MXI "root" mainframe (Model D20 Slave Cluster *2* frame in figure **3)** must have a VXI resource manager in slot 0 (e.g. HP E1405/1406 Command Module).
- A VXI-MXI Bus Extender Module (HP E1482) should be installed in the slot next to the resource manager in the VXI-MXI "root" mainframe (Model D20 Slave Cluster **2** frame in figure *3)* .
- VXI-MXI "extender" frames must have a VXI-MXI **Bus** Extender Module (HP E1482) in slot 0.

HP E1405/E1406 Command Module Set Up

To configure a multi-frame system as a single instrument, the command module must have a user defined Commander/Servant Hierarchy table stored in it using the HP E1405/1406 Command Module VXI:CONFigure:CTABle command. Without this table, the command module of a multiple mainframe system treats the modules of each mainframe as separate instruments because of logical address gaps present between the modules from frame to frame. You can override the command module's algorithm for assigning each mainframe as an idividual instrument by downloading a Commander/Servant Hierarchy table with the CTABle command. This configuration table tells the command module the groups of addresses to be treated as one instrument (even though they are separated by logical address gaps).

This chapter gives an example of connecting three mainframes together with VXI-MXI Extender Modules and provides a program that downloads a configuration table to make the modules of all three mainframes operate as one instrument. Figure *3* lists the logical addresses used in the example.



HP E1450-61603 (3 required)

MXIbus cables and INTX cables between the VXI-MXI Extender Modules and the HP-IB cable to the Command Module are not shown installed for clarity of the diagram. These cables must be installed for an operational system.

Mainframe Logical Addresses:

- HP E1406 = 0 (System Resource Manager)
- HP E1482 = 128 (VXI-MXI "root" mainframe)

Model D20 Slave (Cluster 2):

- HP E1450 = 136
- HP E1451 #1 = 137
- HP E1451 #2 = 138
-
-
- HP E1451 #7 = 143
- HP E1452 = 144

Mainframe Logical Addresses:

- HP E1482 = 64 (VXI-MXI "extender" mainframt,

Model D20 Master (Cluster 0):

- HP E1450 = 72
- HP E1451 #1 = 73
- HP E1451 #2 = 74
-
-
- HP E1451 #9 = 81
- HP E1452 = 82

Mainframe Logical Addresses:

- HP E1482 = 96 (VXI-MXI "extender" mainframe)

Model D20 Slave (Cluster 1):

- HP E1450 = 104
- HP E1451 #1 = 105
- HP E1451 #2 = 106
-
-
- HP E1451 #9 = 113
- HP E1452 = 114

Figure 3. VXI-MXIbus Configuration (3 Frames)

Programming: VXI-MXIbus Configuration

The following example program configures the three-frame system shown in figure **3.** The data for the configuration table **is** contained in the **DATA** lists in lines **920** to 1000. There are two system boot cycles; the first boot cycle reserves memory for the configuration table, the second boot cycle activates the table.

```
10   !Example program for making a "3-frame instrument"
20   INTEGER Ctab(0:127),Mod_count,Cmdr,Sec_addr,Laddr,Tab_idx,Err_num
30   REAL Ctab_addr
40   DIM Err_str$[255]
50   !
60   ASSIGN @Syst TO 80900;EOL CHR$(10) END
70   Default-to = 10
80   ON TIMEOUT SC(@Syst),Default_to GOTO Hpib_to
90   !
100   RESTORE Ctab_data
110   READ Cmdr
120   READ Sec_addr
130   !
140   ! Fill configuration table
150   Mod-count = 0
160   Tab-idx = 1
170   READ Laddr
180   WHILE Laddr > 0
190       Ctab(Tab_idx) = Laddr
200       Tab- idx = Tab-idx + 1
210       Ctab(Tab_idx) = Cmdr
220       Tab- idx = Tab-idx + 1
230       Ctab(Tab_idx) = Sec_addr
240       Tab_idx = Tab-idx + 1
250       Mod_count = Mod-count + 1
260       READ Laddr
270   END WHILE
280   Ctab(0) = BINIOR(Mod_count,256)
290   !
300   ! Adjust table size
310   REDIM Ctab(0: (Mod-count*3))
320   !
330   ! Allocate table space in controller
340   CLEAR @Syst
350   OUTPUT @Syst;"*CLS"
360   OUTPUT @Syst;"DIAG:NRAM:CRE  ";2 + (6*Mod_count)
370   OUTPUT @Syst;"SYST:ERR?"
380   ENTER @Syst;"Err_num;Err_str$
390   IF Err_num < > 0 THEN
400       PRINT Err_num,Err_str$
410       STOP
420   END IF
```

```
430   DISP "Booting system to create table"
440   OUTPUT @Syst;"DIAG:BOOT"
450   ON TIMEOUT SC(@Syst),.2 GOTO Boot_loop1
460 Boot-loop1:   !
470   Stat =SPOLL(@Syst)
480   !
490   ! Download and link table
500   DISP ""
510   ON TIMEOUT SC(@Syst),Default_to GOTO Hpib_to
520   OUTPUT @Syst;"*CLS"
530   OUTPUT @Syst;"DIAG:NRAM:ADDR?"
540   ENTER @Syst;Ctab_addr
550   OUTPUT @Syst;"DIAG:DOWN  ";Ctab_addr;",#0";
560   OUTPUT @Syst USING "W";Ctab(*)
570   OUTPUT @Syst;"SYST:ERR?"
580   ENTER @Syst;Err_num;Err_str$
590   IF Err_num< >0 THEN
600       PRINT "Error due to DIAG:DOWN - -";
610       PRINT Err-num,Err_str$
620       STOP
630   END IF
640   OUTPUT @Syst;"VXI:CONF:CTAB  ";Ctab_addr
650   OUTPUT @Syst;"SYST:ERR?"
660   ENTER @Syst;Err_num;Err_str$
670   IF Err-num< >0 THEN
680       PRINT "Error due to VXI:CONF  - -";
690       PRINT Err_num,Err_str$
700       STOP
710   END IF
720   !
730   ! Do final boot to make table effective
740   DISP "Booting system to install table"
750   OUTPUT @Syst;"DIAG:BOOT"
760   ON TIMEOUT SC(@Syst),.2 GOTO Boot_loop2
770 Boot_loop2:   !
780   Stat_SPOLL(@Syst)
790   DISP""
800   ON TIMEOUT SC(@Syst),Default_to GOTO Hpib_to
810   DISP "Instrument configuration complete"
820   WAIT .5
830   STOP
840   !
850   !
860 Hpib_to:   !
870   PRINT "HPIB at select code ";SC(@Syst);" timed out"
880   STOP
890   !
900   !
```

```
910 Ctab_data:   !
920   DATA 0          !Logical address of instrument's commander
930   !
940   DATA9           !Desired secondary address of instrument
950   !
960   ! Now the list of member logical addresses (terminate with 0 or -1)
970   DATA 72,73,74,75,76,77,78,79,80,81,82
980   DATA 136,137,138,139,140,141 ,142,143,144
990   DATA 104,105,106,107,108,109,110,111,112,113,114
1000   DATA 0
1010   !
1020   !
1030   END
```